

WHAT IS CLAIMED IS:

1. For use with a power converter having a main active clamp
2 circuit associated with a main power switch coupled to a primary
3 winding of a transformer and a rectifier switch coupled to a
4 secondary winding of said transformer, said main power switch
5 configured to conduct during a main conduction period of said power
6 converter and said rectifier switch configured to conduct during an
7 auxiliary conduction period of said power converter, a gate driver,
8 comprising:

9 a DC offset bias circuit, coupled to a secondary winding of
10 said transformer, configured to provide a gate drive signal having
11 a DC bias voltage to a gate terminal of said rectifier switch.

2. The gate driver as recited in Claim 1 further comprising
2 a resistor, coupled in series with said gate terminal of said
3 rectifier switch, configured to extend a transition time of said
4 rectifier switch from a conducting state during said auxiliary
5 conduction period to a non-conducting state.

3. The gate driver as recited in Claim 1 wherein said DC
2 offset bias circuit comprises a battery.

4. The gate driver as recited in Claim 1 wherein said DC
2 offset bias circuit comprises a zener diode.

5. The gate driver as recited in Claim 4 wherein said DC
2 offset bias circuit further comprises a capacitor coupled in
3 parallel to said zener diode.

6. The gate driver as recited in Claim 4 wherein said DC
2 offset bias circuit further comprises a resistor coupled to said
3 zener diode.

7. The gate driver as recited in Claim 1 wherein said
2 rectifier switch is a synchronous rectifier switch.

8. For use with a power converter having a main active clamp
2 circuit associated with a main power switch coupled to a primary
3 winding of a transformer and a rectifier switch coupled to a
4 secondary winding of said transformer, said main power switch
5 conducts during a main conduction period of said power converter
6 and said rectifier switch conducts during an auxiliary conduction
7 period of said power converter, a method of driving said rectifier
8 switch, comprising:
9 coupling a DC offset bias circuit to a secondary winding of
10 said transformer and a gate terminal of said rectifier switch; and
11 providing a gate drive signal having a DC bias voltage via
12 said DC offset bias circuit to a gate terminal of said rectifier
13 switch.

9. The method as recited in Claim 8 further comprising
2 extending a transition time of said rectifier switch from a
3 conducting state during said auxiliary conduction period to a non-
4 conducting state.

10. The method as recited in Claim 8 wherein said DC offset
2 bias circuit comprises a battery to provide said DC bias voltage.

11. The method as recited in Claim 8 wherein said DC offset
2 bias circuit comprises a zener diode.

12. The method as recited in Claim 11 wherein said DC offset
2 bias circuit further comprises a capacitor coupled in parallel to
3 said zener diode, said zener diode and capacitor cooperating to
4 provide said DC bias voltage.

13. The method as recited in Claim 11 further comprising
2 providing a bias current to said zener diode.

14. A power converter, comprising:

2 a main power switch coupled to an input of said power
3 converter that conducts during a main conduction period of said
4 power converter;

5 a main active clamp circuit associated with said main power
6 switch;

7 a transformer having a primary winding coupled to said main
8 power switch;

9 a rectifier coupled to a secondary winding of said transformer
10 and including a rectifier switch that conducts during an auxiliary
11 conduction period of said power converter; and

12 a gate driver, including:

13 a DC offset bias circuit, coupled to a secondary winding
14 of said transformer, that provides a gate drive signal having
15 a DC bias voltage to a gate terminal of said rectifier switch.

15. The power converter as recited in Claim 14 wherein said
2 gate driver further comprises a resistor, coupled in series with
3 said gate terminal of said rectifier switch, that extends a
4 transition time of said rectifier switch from a conducting state
5 during said auxiliary conduction period to a non-conducting state.

16. The power converter as recited in Claim 14 wherein said
2 DC offset bias circuit comprises a battery.

17. The power converter as recited in Claim 14 wherein said
2 DC offset bias circuit comprises a zener diode coupled in parallel
3 to a capacitor, said DC offset bias circuit further comprising a
4 resistor coupled to said zener diode.

18. The power converter as recited in Claim 14 wherein said
2 rectifier switch is a synchronous rectifier switch.

19. The power converter as recited in Claim 14 further
2 comprising an auxiliary active clamp circuit associated with said
3 rectifier switch.

20. The power converter as recited in Claim 19 wherein said
2 auxiliary active clamp circuit, comprises:
3 an auxiliary clamp capacitor, coupled across said rectifier
4 switch, that stores a clamping voltage substantially equal to an
5 off-state voltage of said rectifier switch; and
6 an auxiliary clamp switch, coupled in series with said
7 auxiliary clamp capacitor, that receives a drive signal from a
8 secondary winding of said transformer and conducts during said main
9 conduction period thereby clamping a voltage across said rectifier
10 switch at about said clamping voltage.